Cushman CE-6A Service Monitor
100 Hz Phase Locked Loop Theory of Operation

The following data could not have been presented without the extensive efforts at reverse engineering and circuit analysis undertaken by my brother, Jerry Thorusen, M.S.E.E. and my best friend Richard Thomsen, M.S.E.E. Their patience, long hours and long suffering have been indispensible to this work.

Since I have edited their explanations and comments and interwoven them with my own narrative, any errors or omissions are mine alone. To ensure proper appreciation and credit is given where credit is due, I wish to dedicate this work to them.

Because this work came about as a result of a need to repair a particular problem, certain portions of the circuitry are treated minimally. To completely reverse-engineer and describe a device as complicated as the Cushman CE-6A would require more man-hours than remain in mine and my friends lifetimes. However, it is hoped that this discussion will still be of some help to others to keep their vintage but still very useful CE-6's up and running.

Some of this data was gathered by circuit analysis from the Cushman schematics (principally done by Richard), some by computer simulation (principally done by Jerry) and some by bread-boarding the circuits on a Heathkit Designer system (principally done by myself). The scope camera photos and voltage measurements were made by me in the process of trouble-shooting the instrument.

Again, most of the good stuff comes from Richard and Jerry; the errors and omissions are mine.

James K. Thorusen

April 7, 2015

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As with all phase locked loops, the CE-6A 100 Hz loop is a tail-chasing circuit. All parts of it have to work before the entire system will work. Therefore, when either trouble-shooting the circuit or describing it, the first step is to break the loop. For both this description and the trouble-shooting recommendations and alignment instructions to follow, I have chosen to break the loop at the summing point, designated with the Greek letter Sigma Σ in the loop block diagram (Figure 4-1) on page 4-4 of the manual. It will be helpful to have this diagram, the Cushman theory of operation discussion and the schematics for the various cards involved with the 100 Hz loop ready to hand so that they may be referred to as this discussion progresses.

Please note that while informative, the Cushman theory discussion centers on the circuitry involved on each card. Thus, detailed theory is scattered in several places in the book. I have chosen to follow the signal around the loop which I think gives better continuity to the discussion.

With the loop broken, we will begin our discussion of the VCO, or voltage controlled oscillator. Please refer to the schematic Figure 6-27 on pages 6-119 / 6-120 of the manual for the following discussion. Q20 appears to be a modified Colpitts oscillator, which covers the frequency range of 20 to 20.9999 Mhz. The tunable coil L5 sets the coarse operating frequency of Q20. Fine frequency control is accomplished by varying the bias on a pair of varactor diodes (CR6 and CR7). These diodes are reversed biased; they do not conduct in normal operation. The larger the reverse bias, the further the charge carriers are forced from the junction plane. This is equivalent to moving the plates of a capacitor further apart and so reduces the junction capacitance of the diodes. Thus, these varactors are voltage-controlled capacitors, and therefore allow the oscillator to be tuned by varying their DC bias, creating a VCO, or Voltage Controlled Oscillator.

The output of the VCO is buffered by Q19 and fed to a balanced mixer on the 4500 board (Figure 6-29 on pages 6-127 and 6-128 of the manual). Here it is mixed with a 9.9 MHz reference signal derived from the reference crystal oscillator. The resulting product, in the range of 200 KHz to 1.999 MHz is then fed to the divide-by-N circuitry on the 4100 board (Figure 6-26 on pages 6-113 / 6-114 of the manual). The function of the mixer is straightforward; refer to paragraph 4.58 on page 4-6 of the manual for a more detailed discussion.

The divide-by-N circuitry divides the 200 KHz to 1.9999 MHz signal derived from the mixer on the 4100 board to 100 Hz. The numerical divisor is chosen by the setting of the frequency selector switches on the front panel of the CE-6 to the right of the decimal point. For a more detailed description of the workings of the divide-by-N circuit, refer to paragraphs 4.44 through 4.49 and table 4-1 in the manual on pages 4-4 and 4-5.

HOWEVER! What the manual does not tell you is that the output of the divide-by-N circuitry is always a 20 microsecond duration pulse. This pulse occurs with a repetition rate of 100 Hz when the loop is locked, and faster or slower repetition rates when the VCO is either too high or too low in frequency, respectively. The TIMING of this pulse, i.e. when it occurs with respect to a pulse generated from the reference crystal oscillator, contains the PHASE INFORMATION necessary to lock the loop.

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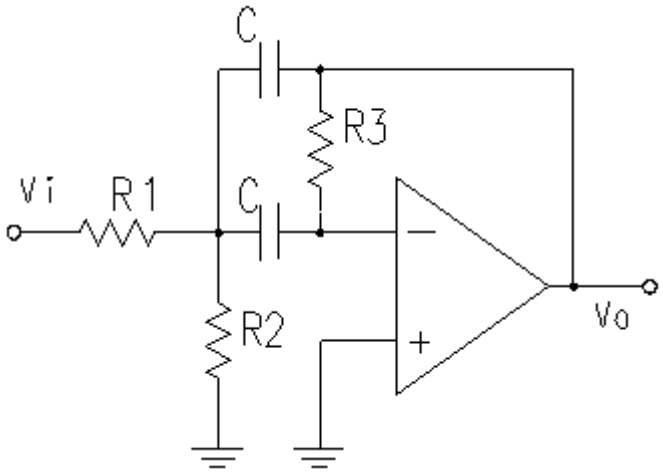
Now we come to the 100 Hz loop filter. As this is where the trouble in my case was located, the circuit will be discussed in more detail. For Cushman's take on it, please refer to paragraph 4.59 on page 4-6 of the manual.

This discussion is pretty good, except that it omits a discussion of R7 and any details of how to set up and align the filter. As said in paragraph 4.59 of the manual, R10 sets the frequency of the active filter consisting of IC3 and its associated components. Note that the values of R3, R6 and R9 are all critical to the frequency response of the filter. It is also important to note that the phase information necessary to lock the loop does NOT pass through the filter! The filter is a go / no-go gate. When the input pulse repetition rate is outside the filter bandwidth, the output is gated to a steady logic 1, which drives the VCO board into "Search" mode (more on this later). When the repetition rate of the pulses is close to 100 Hz, then the 20 microsecond pulses applied to the input of the filter board pass through to the output.

The active filter frequency response closely approximates that given by the following discussion from Swarthmore.edu (http://www.swarthmore.edu/NatSci/echeeve1/Ref/FilterBkgrnd/Filters.html).

If you derive the transfer function of the circuit shown below:

High-Q Bandpass Filter with Op Amp



you will find that it acts as a band-pass filter with:

$$H_o = -\frac{R_3}{2R_1}$$

and the center frequency and bandwidth given by:

Radian frequency	Hertz
$\omega_o = \frac{1}{C\sqrt{(R_1 \| R_2)R_3}}$	$f_o = \frac{\omega_o}{2\pi}$
$\beta = \frac{2}{CR_3}$	$B = \frac{\beta}{2\pi}$

The notation $R_1||R_2$ denotes the parallel combination of R_1 and R_2,

$$R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

.

The output of this filter is a sine wave, even though driven by 20 microsecond pulses; the filter Q ensures that the circuit will "ring" at the resonant frequency. In the absence of R7 and R8, the output sine wave would be symmetrical around zero volts. Adding these components allows the axis of the output sine wave to be shifted with respect to zero volts. The output sine wave is rectified by CR5 and applied to the base of Q5. Pin 7 of IC4 is held high by pull-up resistor R17. When there is sufficient average base current through Q5, pin 7 of IC4 is held low, allowing the 20 microsecond pulses from the divide-by-N circuit to pass on to the VCO board. C32 prevents the pull-up resistor from pulling pin 7 of IC4 high during the intervals between the rectified peaks of the sine wave output from IC3. In the absence of positive-going rectified pulses from the sine-wave output of IC3, R17 pulls pin 7 of IC4 high. When pin 7 of IC4 is high, the output of IC4 leaving the board is locked high, removing the 20 microsecond pulses from the output thus depriving the VCO board of phase information and driving it into "Search" mode.

The turn-on condition for Q5 is established by the number and amplitude of the 100 Hz sine wave peaks passed through the IC3 filter. These peaks must be above two diode drops (CR5 drop and the base-emitter drop of Q5) and contain sufficient energy to allow Q5 to hold the voltage on C32 low against the pull-up from R17. This is where the R7 and R8 resistors come in. By setting the level of the axis of the sine wave output from IC3, they determine whether any of the sine wave peaks will be positive enough to turn on Q5 and further, they determine how many of those peaks will be high enough, since the amplitude of the sine wave will decrease as the filter input frequency departs from 100 Hz. Therefore, the potentiometer R7 effectively sets the filter BANDWIDTH.

The illustration below may help to visualize this:

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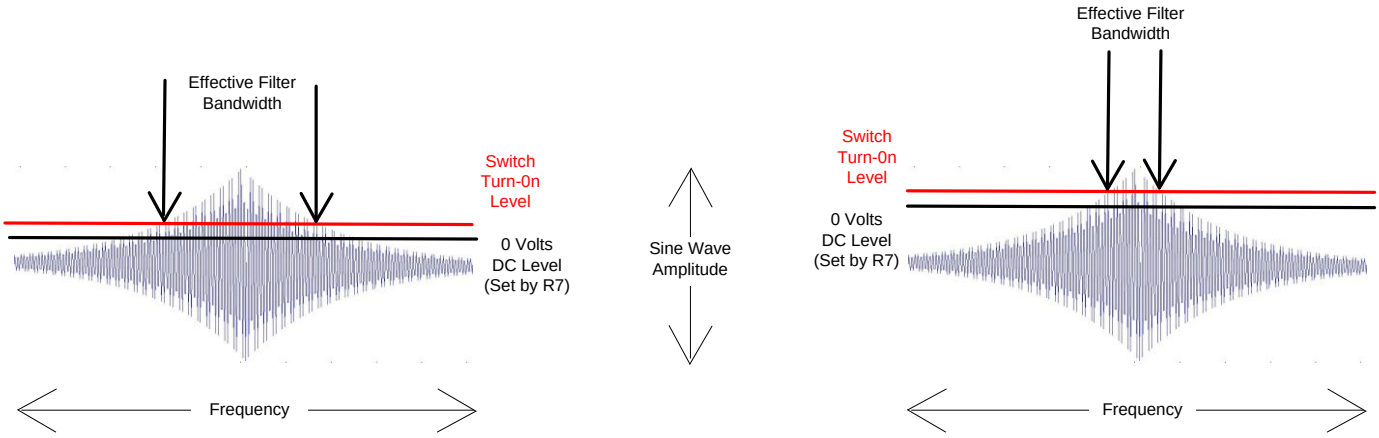

Filter response shown as amplitude of output sine wave versus frequency.

Diagram showing DC Offset versus

Effective Filter Bandwidth

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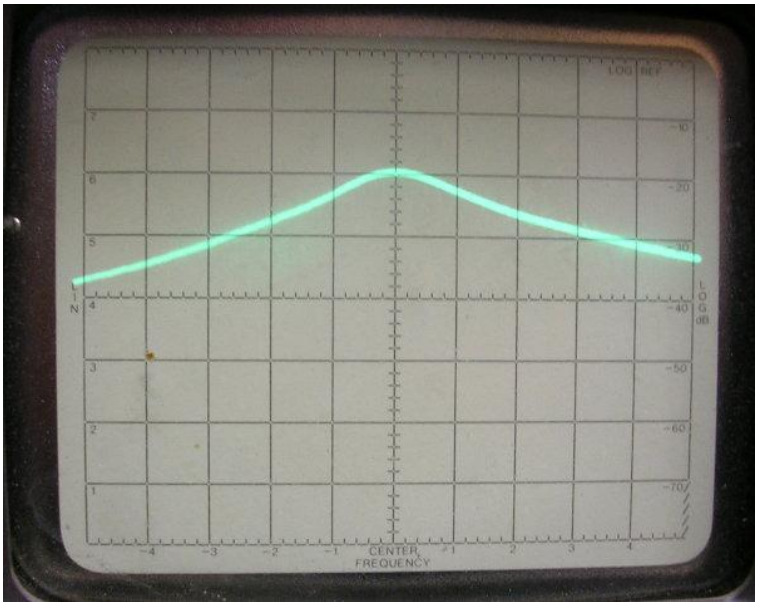
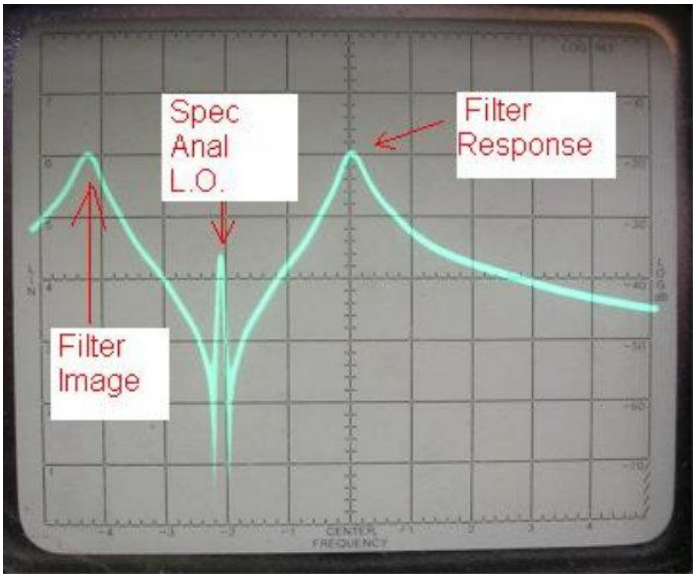
The following scope camera photos are of the frequency response of a mockup filter built on a bread board. The capacitor values were reduced by a factor of 100 to scale the filter response frequency up by 100 to allow easier spectrum analysis.

Here are the spectrum analyzer photos:

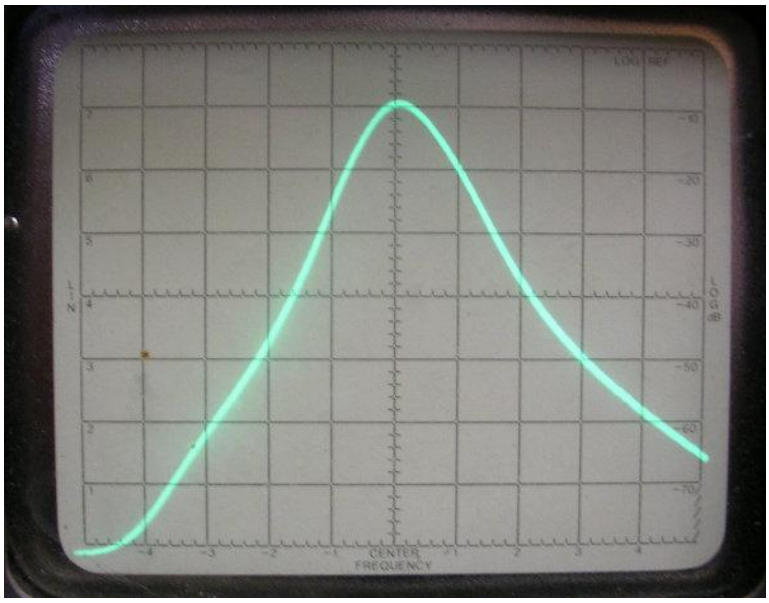
The first one is the filter response with 300 Hz bandwidth, 10 dB / Div, 10 KHz center frequency and 1 KHz / div; scale set to dBm.



This next picture is the filter response with 300 Hz bandwidth, 10 dB / Div, 10 KHz center frequency and 5 KHz / div; scale set to dBm:



The last picture is the filter response with the vertical scale set to 2 dB log so that the frequency response at the 1/2 power (3dB) points can be seen more easily. (Filter response with 300 Hz bandwidth, 2 dB / Div, 10 KHz center frequency and 1 KHz / div; scale set to dBm.):



As you can see, the filter response is slightly asymmetrical. In practice, the filter response is set to maximum at 102 Hz to allow for equal distance between the desired 100 Hz pass and the dropout points, with the bandwidth being set to 20 Hz. As you will note from the above photo, when scaled, this bandwidth is at the approximate 3dB or half-power points at which Q and effective bandwidth are generally defined.

After the loop filter, the 20 microsecond pulses at 100 Hz repetition rate are passed to the VCO board. Also passed to the VCO board are 20% duty cycle fast rise time pulses at a 100 Hz repetition rate derived from the crystal oscillator frequency standard. For a discussion of how this is done, please refer to paragraphs 4.27 through 4.30 on pages 4-2 and 4-3 of the manual. (Note: There is an engineering change to this circuit, but it does not affect the 100 Hz reference pulses sent to the VCO board.)

To aid in understanding the following theory, it is suggested that one refer to the diagram on page 10.

The 100 Hz repetition rate pulses derived from the reference standard are used to generate a ramp voltage on the VCO board. Note that the description given in the Cushman theory in paragraph 4.51 on page 4-5 is incorrect. The ramp is positive-going.

The ramped voltage is used to turn the phase difference information (which is actually a timing difference between the reference pulse that triggers the ramp and the output of the Divide-by-N circuitry) into an error voltage that controls the VCO and locks it to the reference. This is accomplished by taking a sample of the ramp voltage at the time when the Divide-by-N pulse appears. Since the ramp voltage

increases with time, the larger the time difference between the reference pulse which starts the ramp and the Divide-by-N pulse which triggers the sample, the further up the ramp the sample will be and thus the higher the voltage sampled at that particular time. The sample and hold operation is done twice by two very similar circuits before being passed to the differential amplifier consisting of Q9 and Q11, which will be discussed later.

The reason for this dual sample and hold technique lies in the fact that the first sampling pulse from the Divide-by-N circuitry has a finite duration: twenty microseconds. During this time, the ramp voltage increases. Therefore, instead of being a discrete voltage, the output of the first sample and hold is a voltage with a small change over time. Although this change is small due to the short duration of the sampling pulse, if applied directly to the VCO, the result would be a "chirp" in the VCO output frequency during the sampling time.

Therefore, it is necessary to integrate the ramped voltage obtained during the first sample period. This is accomplished by allowing the voltage to be accumulated on C21. After the initial sampling period has ended, the voltage on C21 is steady and is approximately the voltage of the ramp at the end of the first 20 uSecond sampling pulse. This constant value is transferred out of the system and on to the differential amplifier (Q9 and Q11) by the second (delayed) sampling pulse from IC1 pin 14.

Detailed theory of operation of the sample and hold portion of the circuitry follows:

R3, R6, C10, R21, and Q7 make up a constant current source. CR3 is a 4.5V Zener diode, connected to a 20V line. So the voltage at the base of Q7 is 20V minus 4.5V, or 15.5V. The voltage across R21 is 4.5V minus the emitter-base voltage drop of about .6V, or 3.9V, so the max current through Q7 is 3.9V = I * 3.3K, or about 1.18ma.

When the 100Hz reference input signal is high, it drives Q5 on, thus discharging C11. When the 100Hz reference input signal is low, C11 charges with 1.18ma of current, driving TP5 to a ramp from zero volts up towards 15V.

The output of the Divide-by-N circuitry appears at TP3. This is a 20 uSecond positive-going pulse with a 100 Hz repetition rate. When TP3 is low, Q12 is turned off. This allows the base of Q10 to reach the same value as its emitter, pulled up by current through R39 and R41. With its base at the same voltage as its emitter, Q10 is cut off. The collector of Q10 is connected to a minus 12 volt source through R35.

With Q10 not conducting, its collector approaches minus 12 volts. This negative voltage forward biases CR4 and thus is passed through CR4 to the gate of Q8. Thus Q8 is cut off.

When the positive-going pulse from the Divide-by-N circuitry arrives, Q12 is turned on. This pulls the base of Q10 low and it conducts. R39 limits the base current of Q10 to a safe value. R41 limits the collector current of Q12.

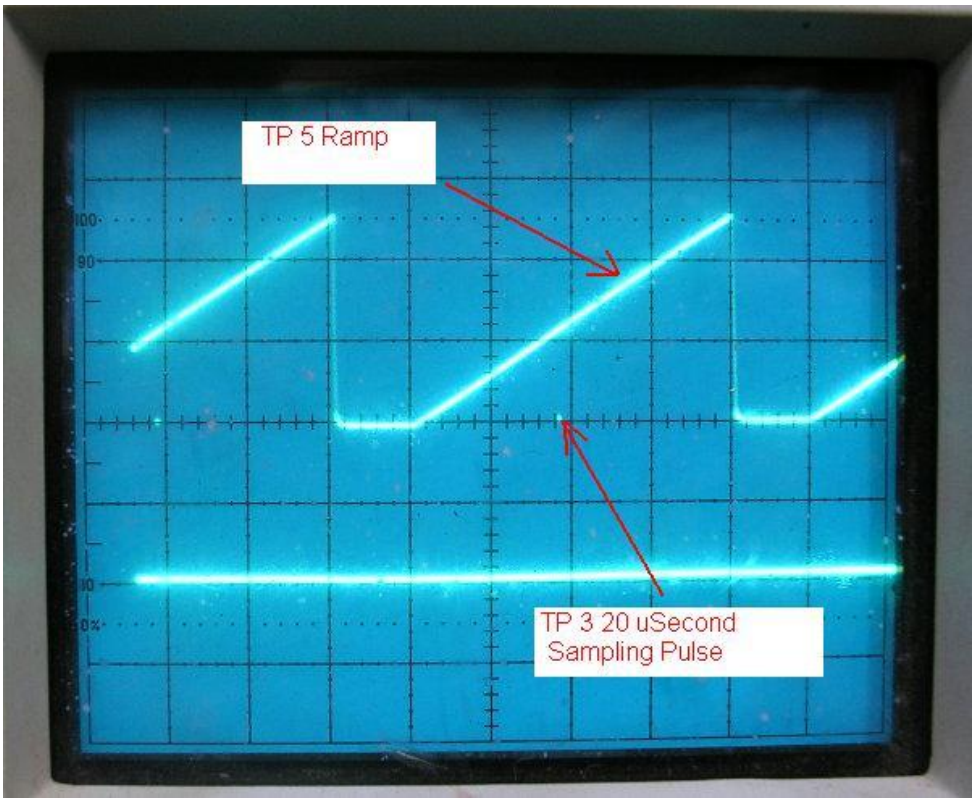
With Q10 conducting, its collector voltage approaches that of its emitter, which is connected to the plus 20 volt buss through a 100 ohm resistor, R34. Thus, there is a large positive voltage present on the collector of Q10. This positive voltage reverse biases CR4, and thus no current can flow through it. With CR4 reverse biased, R24 pulls the gate of Q8 to a voltage that is essentially equal to its source, thus allowing current through to charge C21. C21 thus charges to a voltage that is determined by the amplitude of the ramp generated at TP5 at the time the sampling pulse is present. This constitutes the first sample and hold circuit.

Q15 and Q16 together constitute a DC amplifier. The gate of Q15 presents a high impedance to the stored voltage on C21 and thus the DC amplifier output is representative of that voltage even though current may be drawn from its output.

Q17, Q18 and Q22 form another sample and hold gate, very similar to the first one formed by Q8, Q10 and Q12 discussed above. This sample is taken immediately after the first sample, triggered by a delayed sampling pulse sourced from IC1, pin 14. IC1 is a "one-shot" delay circuit that creates a second sampling pulse that is derived from the falling edge of the first one which is the output of the Divide-by-N circuitry. Thus, this pulse immediately follows the first sampling pulse in time and samples the voltage on C21 (buffered by Q15 and Q16) as soon as it has settled.

During the second sampling period, Q17 conducts, passing the output of the DC amplifier (Q15 and Q16) to the second storage capacitor, C32. This voltage controls the current through Q24 and thus controls the voltage presented to point "**A**" which is passed to the differential amplifier (Q9 and Q11).

The following scope camera photo and timing diagram will be helpful in understanding the sample and hold theory.



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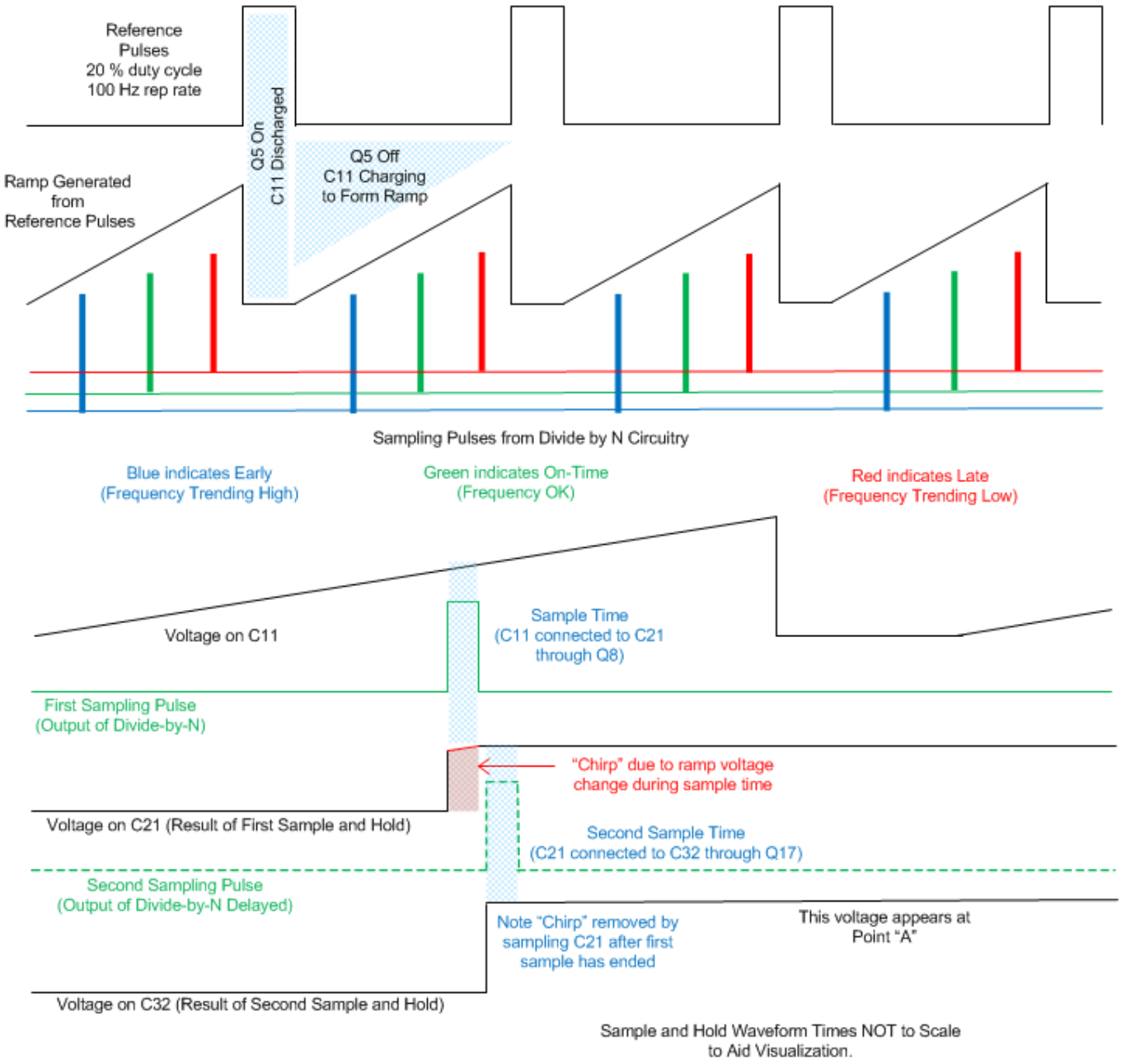

The differential amplifier circuit consists of Q6, Q9, Q11 and Q14. The operation of this circuit is discussed in the Cushman manual, paragraph 4.53 on page 4-5. The purpose of the circuit is to further buffer and level translate the voltage from the sample and hold circuits before application to the VCO and also to form a "search" oscillator to drive the VCO back and forth through its frequency range when the system has deviated so far from its desired lock frequency that the 100 Hz loop filter has inhibited the presence of the Divide-by-N pulses. This amplifier is NOT an inverting amplifier... i.e. as the voltage on point "A" increases, so does the voltage on the collector of Q11, which is delivered to the summing point through R55.

On page 4-4 of the manual you will find a block diagram of the 100 Hz loop, Figure 4-1. In this diagram, you will find a block labeled with the Greek letter Sigma (Σ). This point is a summing point for all the voltages that try to control the VCO. Physically, it is the junction of R17, R18, R19, R20, R28, R29, R37 and R55 on Figure 6-27, the VCO (4300 board) schematic on page 6-119 / 6-120.

There are two voltages that are summed at this point. One is from the sample and hold circuitry after being buffered by the differential amplifier (Q9 and Q11) and the other is from a Ladder Digital-to-Analog converter circuit. This Ladder D-to-A consists of the 100 KHz. rotary selector switch on the front panel and transistors Q1 through Q4 and their associated circuitry. Depending on the position of the 100 KHz. rotary switch, various combinations of the transistors Q1 through Q4 are switched on or off. The resulting output voltage appears at the summing point and is of the approximate magnitude required to drive the VCO to the frequency selected by the 100 KHz. switch. This enables the phase locked loop to achieve lock faster.

Now, we close the loop.

The voltage at the summing point is applied to the varactors in the VCO through Q13, which functions as both an emitter-follower and a low-pass filter. As this voltage goes more positive, the capacitance of the varactor diodes is reduced and the frequency of the VCO is raised. As this voltage goes lower, the capacitance of the varactors is raised and the VCO frequency goes lower. Since this voltage is principally derived from the output of the sample and hold circuitry which converts the phase (timing) difference between the standard and the Divided-by-N output frequency into a voltage, the loop is closed and the output frequency is locked to the standard.